## **CLAIMS**

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

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\	1. A method of forming a field effect transistor (FET) transistor, comprising
	providing a substrate;
	forming a layer on the substrate, the layer having a side surface;
	forming an epitaxial channel on the side surface, the channel having a
	first sidewall;
	removing the layer for exposing a second sidewall of the channel;
	forming source and drain regions coupled to ends of the first channel
	and
	forming a gate adjacent to at least one of the sidewalls of the channe
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↑ 2. A field effect transistor (FET) comprising:

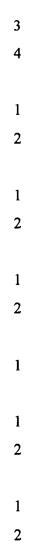
a substrate;

a source region and a drain region in the substrate, each of said source region and said drain region having a top, bottom and at least two side diffusion surfaces, the source and drain regions separated by an epitaxially grown channel region having a top, bottom and side channel surfaces substantially coplanar with corresponding ones of the diffusion surfaces;

a gate adjacent the top and the side channel surfaces and electrically insulated from the top and side channel surfaces; and

the gate comprising a planar top surface, the planar top surface having a contact for receiving a gate control voltage for controlling the FET.

3. The FET as recited in claim 2, wherein the source and drain have a contact for receiving a control voltage for controlling the FET.



4. The FET as recited in claim 2	, wherein the gate is substantially	centered
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- between and substantially parallel to said source region and said drain region.
- 5. The FET as recited in claim 2, further comprising a silicide layer that
- 2 contacts a top surface of said gate.
- 6. The FET as recited in claim 2, further comprising a dielectric layer that
- 2 contacts a first side end and a second side end of said gate.
- 7. The FET as recited in claim 2, further comprising a dielectric that contacts
- 2 side surfaces of the channels.
- 8. The FET as recited in claims 2, where the gate is comprised of polysilicon.
- 9. The FET as recited in claim 2, wherein the channel is approximately one
- 2 fourth of a length of the FET.
- 1 10. The FET as recited in claim 2, further comprising a dielectric material in
- 2 the gate for electrically separating the gate into two electrically isolated
- portions, each having a substantially coplanar top surface and a contact pad on
- 4 each respective substantially coplanar top surface.
- 1 11. The FET as recited in claim 2, wherein said epitaxial channel is formed of
- a combination of Group IV elements.
- 1 12. The FET as recited in claim 2, wherein said epitaxial channel is formed of
- an alloy of silicon and a Group IV element.

1	13. The FET as recited in claim 2, wherein said epitaxial channel is formed of
2	an alloy of silicon and at least one of germanium and carbon.
1	14. A method for forming a double gated field effect transistor (FET),
2	comprising the steps of:
3	forming on a substrate a first and a second epitaxially grown channels;
4	etching areas within a silicon layer to form a source and a drain,
5	wherein a side surface of the source and the drain contact opposing end
6	surfaces of the first and second epitaxially grown channels; and
7	forming a gate that contacts a top surface and two side surfaces of the
8	first and second epitaxially grown channels and a top surface of the substrate.
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1	15. The method as recited in claim 14, wherein the forming step comprises the
2	steps of:
3	forming first and second silicon lines, each end of the silicon lines
4	contact an end of the source and the drain;
5	forming an etch stop layer on an exposed side surface of each of the
6	first and second silicon lines;
7	epitaxially growing first and second silicon layers on each etch stop
8	layer;
9	etching away the first and second silicon lines and etch stop layers;
10	filling areas surrounding the first and second epitaxially grown silicon
11	layers and between the source and the drain with an oxide fill;
12	etching a portion of the oxide fill to form an area that defines a gate,
13	wherein the area that defines the gate is substantially centered between and
14	substantially parallel to the source and the drain; and
15	depositing a material to form a gate.

23. The method as recited in claim 14, wherein the gate material is polysilicon.

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